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Question Paper Code : 41217

B.E./B.Tech. DEGREE EXAMINATION, NOVEMBER/DECEMBER 2015.

Sixth Semester

Electronics and Communication Engineering

EC 1354 — VLSI DESIGN

(Common to Electrical and Electronics Engineering)

(Regulation 2008)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define threshold voltage of MOS transistor.

2. Draw a small signal model for a MOS transistor.

3. Sketch the stick diagram for a tri-state buffer.

4. Draw the CMOS circuit for the following logic equation $f = \overline{a \cdot b + c \cdot d}$, using smallest number of transistor.

5. Write a short note on charge sharing.

6. Why parasitic delay calculation is important in CMOS circuits?

7. Mention the levels at which testing in a chip can be done.

8. Design a set of CMOS gates to implement the sum function.

9. List the various types of design styles in verilog HDL.

10. Write an expression to generate and propagate signals in a circuit using verilog HDL.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the SOI fabrication process of CMOS transistor. (10)

(ii) Derive the design equations for MOS devices. (6)

Or

(b) (i) Explain the operation of NMOS Enhancement transistor. (6)

(ii) Explain the second order effects with their equations. (10)

12. (a) (i) An inverter uses FETs with β_n = 2.1 mA/v2 and β_p = 1.8 mA/v2. The threshold voltages are given as V_{Tn} = 0.60 V and V_{TP} = –0.70 V and the power supply has a value of V_{DD} = 5V. The parasitic FET capacitance at the output node is estimated to be C_{FET} = 74 fF.

(1) Find the midpoint voltage V_M.

(2) Find the values of R_n and R_p.

(3) Calculate the rise and fall times at the output when $C_L = 0$.

(4) Calculate the rise and fall times at the output when the external load of value C_L = 115 fF is connected to the output. (8)

(ii) Discuss the DC and transient characteristics of CMOS inverter. (8)

Or

(b) (i) Sketch the VTC of a CMOS inverter and explain the different regions of operation. (8)

(ii) Explain the concept of dynamic CMOS design. (8)

13. (a) (i) Analyze the CMOS inverter circuit driving the large capacitance loads. (10)

(ii) Discuss the transistor sizing for the performance in combinational networks in brief. (6)

Or

(b) Describe the resistance and capacitance estimation calculation in a CMOS circuit with proper loads and drivers.

14. (a) (i) Explain the physical design flow of VLSI system. (8)

(ii) Discuss the objectives and guidelines for effective power and clock distributions of CMOS system. (8)

Or

(b) What are the different CMOS testing methods? Discuss any two methods.

15. (a) (i) Design a 4-bit ripple carry adder using behavioral model and write the Verilog HDL code to realize the circuit function. (10)

(ii) Explain any five operators used in Verilog HDL with specific examples. (6)

Or

(b) (i) Design a priority encoder using structural model and write the Verilog HDL code to realize the circuit function. (10)

(ii) Write a verilog HDL code for 4 bit magnitude comparator. (6)